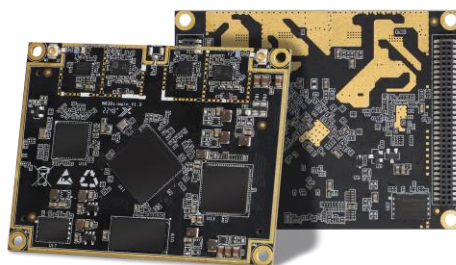


R320M Specification

Wi-Fi6 SOM Module



Introduction

R320M is a highly integrated embedded WIFI6 wireless AP/client module that can be used in conjunction with a customized motherboard to form a complete WIFI6 wireless AP/client product.

The product supports dual independent serial ports and 5 gigabit Ethernet ports, which can meet application scenarios such as AGV, robots, and industrial monitoring. The working temperature can reach -20 °C~+70 °C.

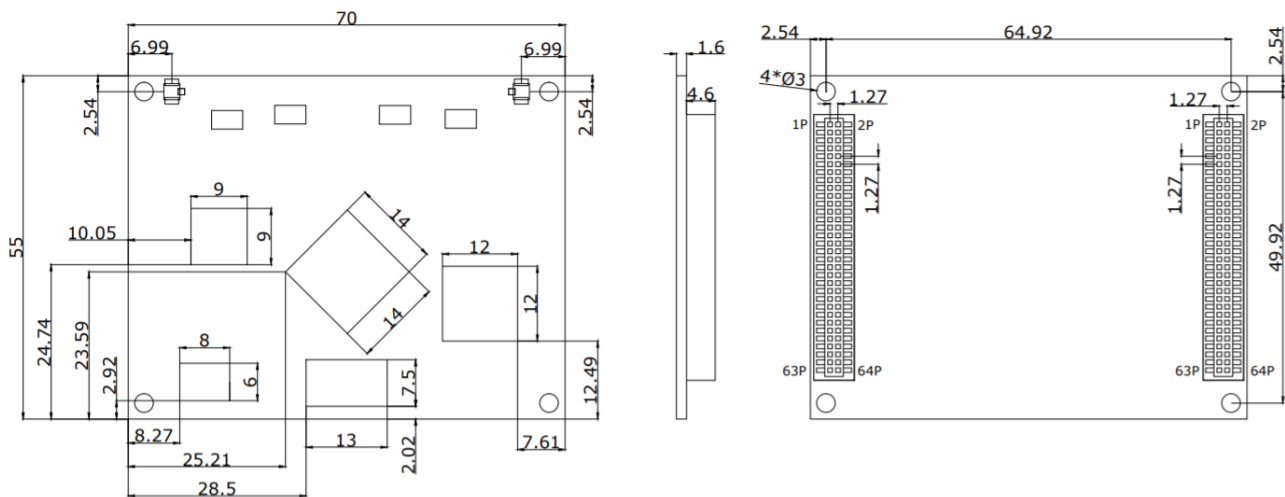
Under the premise of meeting communication speed, a 2 * 2 dual band antenna is adopted to support a design of 2.4GHz+5.8GHz, greatly reducing space occupation. It is an ideal core module for developing products such as commercial APs, industrial routers, and serial servers.

Product Features

- Supports Wi Fi IEEE 802.11a/b/g/n/ac/ax protocol
- Supports 5*Gigabit ports, 1*WAN and 4*LAN
- Supports 1*USB2.0, 1*PCIE2.0/USB3.0(Customized)
- Dual independent serial port design
- Supports 1024QAM modulation technology, increasing data capacity by 50%
- Supporting OFDMA and MU-MIMO technologies, wireless internet access without queuing, reducing latency
- 2.4GHz and 5GHz share antenna interfaces, IPEX 1 connector, saving space

Dimension

Unit: mm



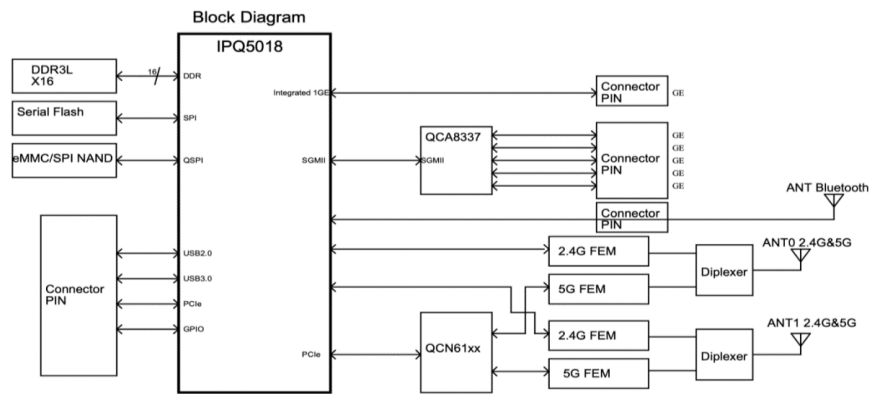
Specifications

Hardware parameter	
Chipset	IPQ5018(Dual-core ARM Cortex-A53 at 1.0 GHz)+QCN6102
Memory	512MB (support 256MB to 1GB) , DDR3L SDRAM ,800 MHz clock rate; 1600 MHz data rate
FLASH	SPI NAND 128MB (up to256MB) ; SPI NOR 8MB (up to 32MB)
NPU	One NPU that consists of 12 threaded programmable engines (UBI32 core), running at 1.0 GHz.
Ethernet	5GE
Antenna	2*IPEX connectors
BT	BT 5.1

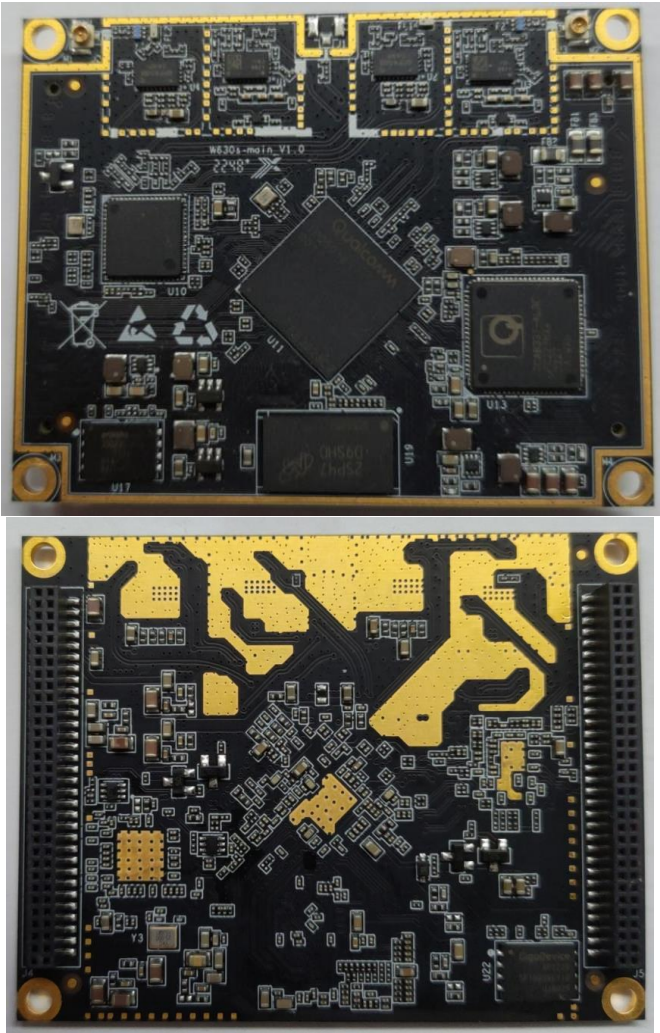
Power supply	6V-16V	
Power consumption	≤10W	
PCBA size	70* 55 * 1.6 mm	
Operating temperature and humidity	-20~70°C, 10% ~ 90% without condensation	
Storage humidity	-40~75°C, 5% ~ 95% without condensation	
WLAN Interface		
Technical standard	IEEE 802.11a/b/g/n/ac/ax	
Frequency band	2.4GHz-2.483GHz 5.15-5.25GHz, 5.25GHz-5.35GHz, 5.725GHz-5.850GHz	
Wi-Fi Spatial flow	2x2+2x2	
2.4GHz Max PHY rate	573.5Mbps	
5GHz Max PHY rate	2474Mbps	
Modulation Type	OFDM:BPSK@6/9Mbps, QPSK@12/18Mbps, 16QAM@24Mbps, 64QAM@48/54Mbps DSSS : DBPSK@1Mbps, DQPSK@2Mbps, CCK@5.5/11Mbps MIMO-OFDM : MCS 0-31 MIMO-OFDM(11ac): MCS 0-9 MIMO-OFDM(11ax): MCS 0~11	
Wireless encryption	WEP (64 or 128) WPA/WPA2/WPA3 personal & enterprise (IEEE 802.1X/RADIUS、TKIP、AES)	
Other interface		
Expand interface	1 x PCIe 2.0 X1 / 1 x USB 3.0	
	1 x USB 2.0	
Miscellaneous interfaces	2*UART, n*GPIO	
RF Parameters		
	2.4GHz	5GHz
TX Power	16 dBm @ MCS11 HE160 -43dB 18 dBm @ MCS11 HE80 -47dB 24 dBm @ MCS9HT40 -35dB 24 dBm @ MCS7 HT20/HT40 -30dB 26 dBm @ MCS0 HT20	16 dBm @ MCS11 HE160 -47dB 20 dBm @ MCS11 HE40 -43dB 23 dBm @ MCS9 HT40 -35dB 23 dBm @ MCS7 HT20/HT40 -30dB 25 dBm @ MCS0 HT20
RX Sensitivity	2.4GHz	5GHz
	-69 dBm @ VHT40/MCS9/2SS -63 dBm @ VHT40/MCS11/2SS -68 dBm @ HE40/MCS9/2SS	-65 dBm @ VHT80/MCS9/2SS -59 dBm @ VHT80/MCS11/2SS -64 dBm @ HE80/MCS9/2SS

	-63 dBm @ HE40/MCS11/2SS	-58 dBm @ HE80/MCS11/2SS
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Block Diagram



Picture

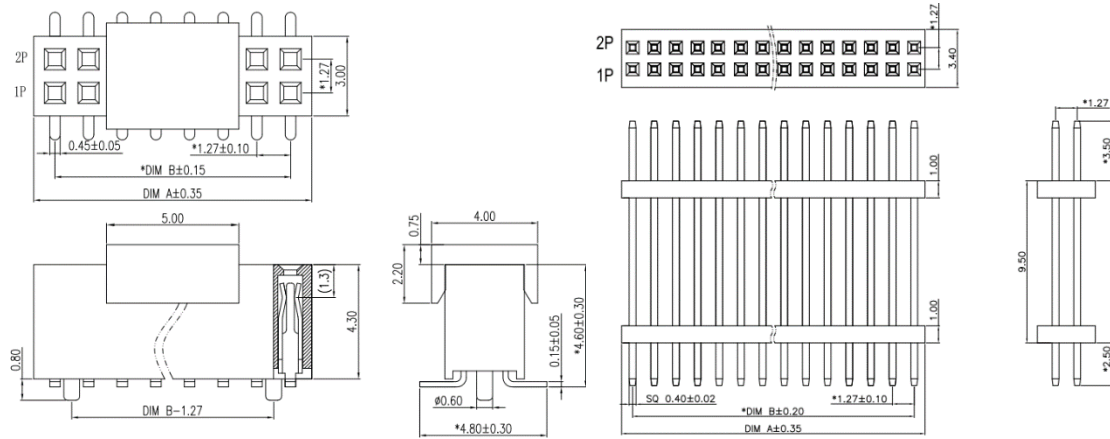


Pin Definition

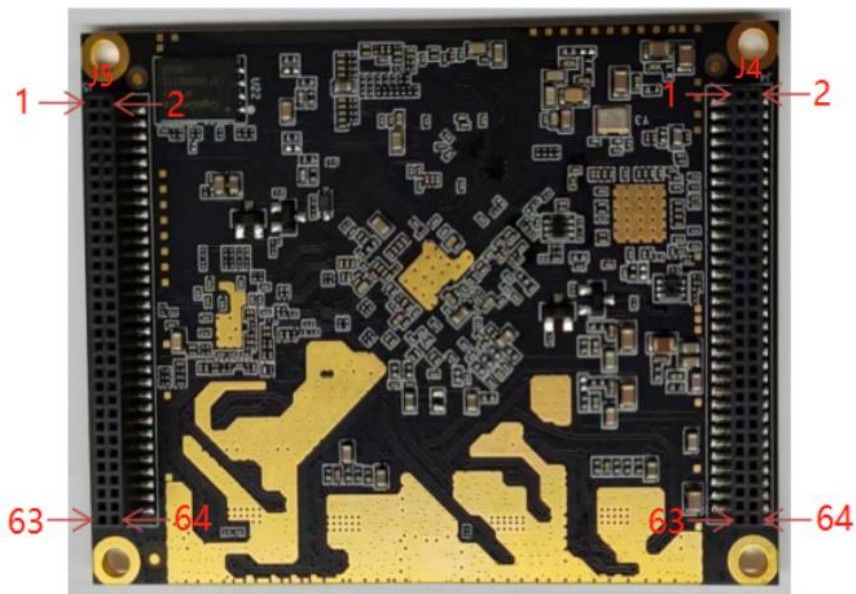
Explanation of seat and positioning holes

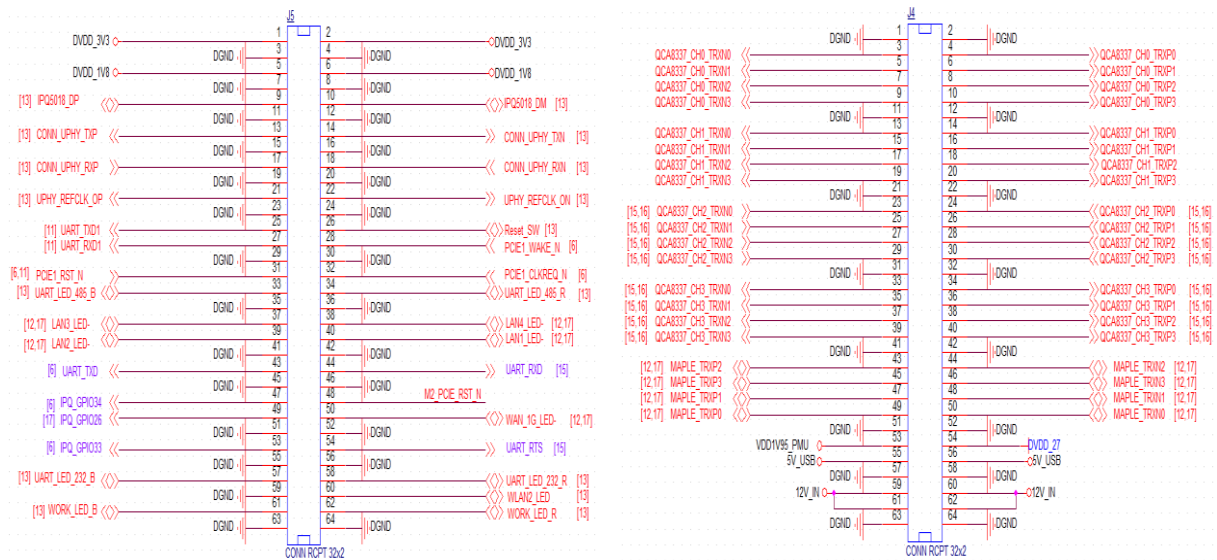
1	seat J4	seat 2*32, pin pitch 1.27mm, seat high 4.3mm, square hole 0.4mm*0.4mm	—
2	seat J5	seat 2*32, pin pitch 1.27mm, seat high 4.3mm, square hole 0.4mm*0.4mm	—
3	positioning holes	The diameter of the positioning installation hole is 2.9mm, Screw suitable for M3	Four positioning holes with the same specifications

Pin specifications corresponding to J4 and J5 in the row



Pin Definition View:





Pin Definition for J4 Seat (1-64)

number	Pin Name	illustrate
1-2,11-12,21-22,31-32,41-42,51,52,57-58,63-64	DGND	Ground
3	QCA8337_CH0_TRXN0	PORT0_0,1000M Ethernet interface data differential signal negative terminal
4	QCA8337_CH0_TRXP0	PORT0_0,1000M Ethernet interface data differential signal positive end
5	QCA8337_CH0_TRXN1	PORT0_1,1000M Ethernet interface data differential signal negative terminal
6	QCA8337_CH0_TRXP1	PORT0_1,1000M Ethernet interface data differential signal positive end
7	QCA8337_CH0_TRXN2	PORT0_2,1000M Ethernet interface data differential signal negative terminal
8	QCA8337_CH0_TRXP2	PORT0_2,1000M Ethernet interface data differential signal positive end
9	QCA8337_CH0_TRXN3	PORT0_3,1000M Ethernet interface data differential signal negative terminal
10	QCA8337_CH0_TRXP3	PORT0_3,1000M Ethernet interface data differential signal positive end
13	QCA8337_CH1_TRXN0	PORT1_0,1000M Ethernet interface data differential signal negative terminal
14	QCA8337_CH1_TRXP0	PORT1_0,1000M Ethernet interface data differential signal positive end
15	QCA8337_CH1_TRXN1	PORT1_1,1000M Ethernet interface data differential signal negative terminal
16	QCA8337_CH1_TRXP1	PORT1_1,1000M Ethernet interface data differential signal positive end
17	QCA8337_CH1_TRXN2	PORT1_2,1000M Ethernet interface data differential signal negative terminal
18	QCA8337_CH1_TRXP2	PORT1_2,1000M Ethernet interface data differential signal positive end
19	QCA8337_CH1_TRXN3	PORT1_3,1000M Ethernet interface data differential signal negative terminal
20	QCA8337_CH1_TRXP3	PORT1_3,1000M Ethernet interface data differential signal positive end
23	QCA8337_CH2_TRXN0	PORT2_0,1000M Ethernet interface data differential signal negative terminal
24	QCA8337_CH2_TRXP0	PORT2_0,1000M Ethernet interface data differential signal positive end
25	QCA8337_CH2_TRXN1	PORT2_1,1000M Ethernet interface data differential signal negative terminal
26	QCA8337_CH2_TRXP1	PORT2_1,1000M Ethernet interface data differential signal positive end
27	QCA8337_CH2_TRXN2	PORT2_2,1000M Ethernet interface data differential signal negative terminal
28	QCA8337_CH2_TRXP2	PORT2_2,1000M Ethernet interface data differential signal positive end
29	QCA8337_CH2_TRXN3	PORT2_3,1000M Ethernet interface data differential signal negative terminal
30	QCA8337_CH2_TRXP3	PORT2_3,1000M Ethernet interface data differential signal positive end
33	QCA8337_CH3_TRXN0	PORT3_0,1000M Ethernet interface data differential signal negative terminal

number	Pin Name	illustrate
34	QCA8337_CH3_TRXP0	PORT3_0,1000M Ethernet interface data differential signal positive end
35	QCA8337_CH3_TRXN1	PORT3_1,1000M Ethernet interface data differential signal negative terminal
36	QCA8337_CH3_TRXP1	PORT3_1,1000M Ethernet interface data differential signal positive end
37	QCA8337_CH3_TRXN2	PORT3_2,1000M Ethernet interface data differential signal negative terminal
38	QCA8337_CH3_TRXP2	PORT3_2,1000M Ethernet interface data differential signal positive end
39	QCA8337_CH3_TRXN3	PORT3_3,1000M Ethernet interface data differential signal negative terminal
40	QCA8337_CH3_TRXP3	PORT3_3,1000M Ethernet interface data differential signal positive end
43	MAPLE_TRXP2	PORT4_2,1000M Ethernet interface data differential signal positive end
44	MAPLE_TRXN2	PORT4_2,1000M Ethernet interface data differential signal negative terminal
45	MAPLE_TRXP3	PORT4_3,1000M Ethernet interface data differential signal positive end
46	MAPLE_TRXN3	PORT4_3,1000M Ethernet interface data differential signal negative terminal
47	MAPLE_TRXP1	PORT4_1,1000M Ethernet interface data differential signal positive end
48	MAPLE_TRXN1	PORT4_1,1000M Ethernet interface data differential signal negative terminal
49	MAPLE_TRXP0	PORT4_0,1000M Ethernet interface data differential signal positive end
50	MAPLE_TRXN0	PORT4_0,1000M Ethernet interface data differential signal negative terminal
53	VDD1V95_PMU	Transformer intermediate tap 1.95V voltage
54	DVDD_27	Positive pole of LAN port indicator light
55-56	5V_USB	Power supply for USB HUB chip and serial port chip
59-62	12V_IN	Module input 7.5V voltage (DC6V~16V)

Pin Definition for J5 Seat (1-64)

number	Pin Name	illustrate
1-2	DVDD_3V3	Power supply for indicator lights, isolation, and level conversion chips
3-4,7-8,11-12,15-16,19-20,23-24,29-30,35-36,41-42,45-46,51-52,55-56,59,63-64	DGND	Ground
5-6	DVDD_1V8	GPIO pull-down and level conversion chip power supply
9	IPQ5018_DP	USB2.0 Differential data line data positive end, Scalable USB device
10	IPQ5018_DM	USB2.0 Differential data line transmission negative terminal, Scalable USB device
13	CONN_UPHY_TXP	PCIE2.0 or USB3.0 Differential data line data positive end, Scalable 5G module
14	CONN_UPHY_TXN	PCIE2.0 or USB3.0 Differential data line transmission negative terminal, Scalable 5G module
17	CONN_UPHY_RXP	PCIE2.0 or USB3.0 Differential data line data positive end, Scalable 5G module
18	CONN_UPHY_RXN	PCIE2.0 or USB3.0 Differential data line transmission negative terminal, Scalable 5G module
21	UPHY_REFCLK_OP	PCIE2.0 or USB3.0 Differential data line data positive end, Scalable 5G module
22	UPHY_REFCLK_ON	PCIE2.0 or USB3.0 Differential data line transmission negative terminal, Scalable 5G module
25	UART_TXD1	Serial port output
26	Reset_SW	restore factory settings

number	Pin Name	illustrate
27	UART_RXD1	Serial port input
28	PCIE1_WAKE_N	PCIE2.0 WAKE-UP SIGNAL
31	PCIE1_RST_N	PCIE2.0 RESET
32	PCIE1_CLKREQ_N	PCIE2.0 Reference clock signal
33	UART_LED_485_B	RS485 Communication serial port indicator light (blue) GPIO38
34	UART_LED_485_R	RS485 Communication serial port indicator light (red) GPIO46
37	LAN3_LED-	LAN3 LED
38	LAN4_LED-	LAN4 LED
39	LAN2_LED-	LAN2 LED
40	LAN1_LED-	LAN1 LED
43	UART_TXD	Debugging serial port output
44	UART_RXD	Serial port input for debugging
47	IPQ_GPIO34	IC2_CLK data
48	M2_PCIE_RST_N	GPIO35 Can connect 5G module reset signal
49	IPQ_GPIO26	Choose between GPIO26 and WAN port indicator lights
50	WAN_1G_LED-	WAN LED
53	IPQ_GPIO33	IC2_CLK clock
54	UART_RTS	Ground
57	UART_LED_232_B	RS232 Communication serial port indicator light (blue) GPIO31
58	UART_LED_232_R	RS232 Communication serial port indicator light (red) GPIO32
60	WLAN2_LED	WIFI LED GPIO30
61	WORK_LED_B	Running status LED (blue) GPIO27
62	WORK_LED_R	Running status LED(red) GPIO28

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